Logic level TOPFET PIP3107-D

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in **TOPFET2** technology assembled in a 3 pin surface mount plastic package.

APPLICATIONS

General purpose switch for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- TrenchMOS output stage
- Current limiting
- Overload protection
- Overtemperature protection
- Protection latched reset by input
- 5 V logic compatible input level
- Control of output stage and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		16	A
P_D	Total power dissipation		65	W
T_j	Continuous junction temperature		150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance		50	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

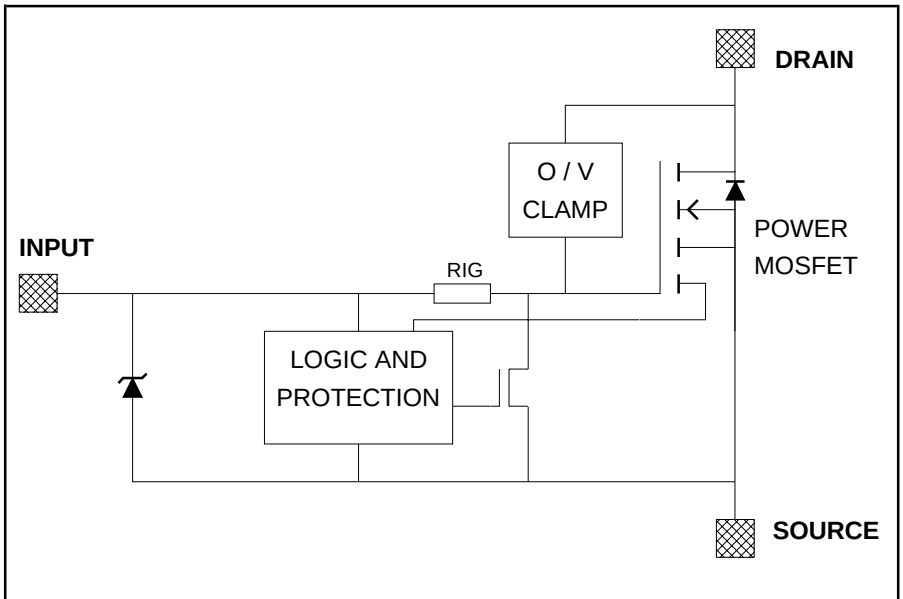
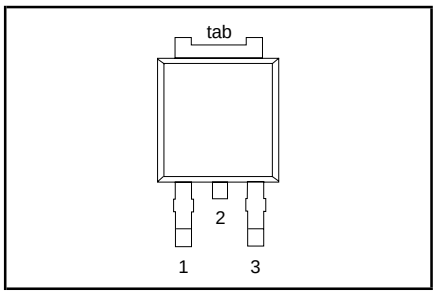


Fig.1. Elements of the TOPFET.

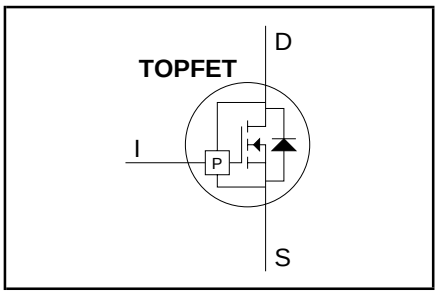
PINNING - SOT428

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
I_D	Continuous drain current	V_{IS} = 5 V; T_{mb} = 25 ˚C	-	self - limited	A
I_D	Continuous drain current	V_{IS} = 5 V; $T_{mb} \leq 125$ ˚C	-	16	A
I_I	Continuous input current	-	-5	5	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-10	10	mA
P_D	Total power dissipation	$T_{mb} \leq 25$ ˚C	-	65	W
T_{stg}	Storage temperature	-	-55	175	˚C
T_j	Continuous junction temperature[2]	normal operation	-	150	˚C
T_{sold}	Case temperature	during soldering	-	260	˚C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Inductive load turn-off	I_{DM} = 16 A; $V_{DD} \leq 20$ V			
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ ˚C	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ ˚C; f = 250 Hz	-	32	mJ

OVERLOAD PROTECTION LIMITING VALUE

With an adequate protection supply provided via the input pin, TOPFET can protect itself from two types of overload - overtemperature and short circuit load.

SYMBOL	PARAMETER	REQUIRED CONDITION	MIN.	MAX.	UNIT
V_{DS}	Drain source voltage[3]	4 V $\leq V_{IS} \leq$ 5.5 V	0	35	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.75	1.92	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB	-	70	-	K/W

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 All control logic and protection functions are disabled during conduction of the source drain diode.

OUTPUT CHARACTERISTICS

Limits are for -40˚C ≤ T_{mb} ≤ 150˚C; typicals are for T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Off-state	V_{IS} = 0 V				
$V_{(CL)DSS}$	Drain-source clamping voltage	I_D = 10 mA	50	-	-	V
		I_{DM} = 2 A; t_p ≤ 300 µs; δ ≤ 0.01	50	60	70	V
I_{DSS}	Drain source leakage current	V_{DS} = 40 V	-	-	100	µA
		T_{mb} = 25 ˚C	-	0.1	10	µA
	On-state	I_{DM} = 6 A; t_p ≤ 300 µs; δ ≤ 0.01				
$R_{DS(ON)}$	Drain-source resistance	V_{IS} ≥ 4.4 V	-	-	95	mΩ
		T_{mb} = 25 ˚C	-	36	50	mΩ
		V_{IS} ≥ 4 V	-	-	100	mΩ
		T_{mb} = 25 ˚C	-	39	55	mΩ

OVERLOAD CHARACTERISTICS

-40˚C ≤ T_{mb} ≤ 150˚C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load	V_{DS} = 13 V				
I_D	Drain current limiting	V_{IS} = 5 V; T_{mb} = 25˚C	16	24	32	A
		4.4 V ≤ V_{IS} ≤ 5.5 V	12	-	36	A
		4 V ≤ V_{IS} ≤ 5.5 V	8	-	36	A
	Overload protection	V_{IS} = 5 V;T_{mb} = 25˚C				
$P_{D(TO)}$	Overload power threshold	device trips if P_D > $P_{D(TO)}$	40	120	160	W
T_{DSC}	Characteristic time	which determines trip time[1]	200	350	600	µs
	Overtemperature protection					
$T_{j(TO)}$	Threshold junction temperature[2]		150	170	-	˚C

1 Trip time $t_{d\,sc}$ varies with overload dissipation P_D according to the formula $t_{d\,sc} \approx T_{DSC} / \ln[\, P_D / P_{D(TO)} \,]$.

2 This is independent of the dV/dt of input voltage V_{IS}.

INPUT CHARACTERISTICS

The supply for the logic and overload protection is taken from the input.
Limits are for -40˚C ≤ T_{mb} ≤ 150˚C; typicals are for T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		0.6	-	2.4	V
			T_{mb} = 25˚C	1.1	1.6	2.1	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	220	400	µA
			V_{IS} = 4 V	80	195	330	µA
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	200	400	650	µA
			V_{IS} = 3 V	130	250	430	µA
V_{ISR}	Protection reset voltage[1]	reset time t_r ≥ 100 µs		1.5	2	2.9	V
t_{lr}	Latch reset time	V_{IS1} = 5 V, V_{IS2} < 1 V		10	40	100	µs
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA		5.5	-	8.5	V
R_{IG}	Input series resistance[2] to gate of power MOSFET		T_{mb} = 25˚C	-	33	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 ˚C; V_{DD} = 13 V; resistive load R_L = 4 Ω. Refer to waveform figure and test circuit.

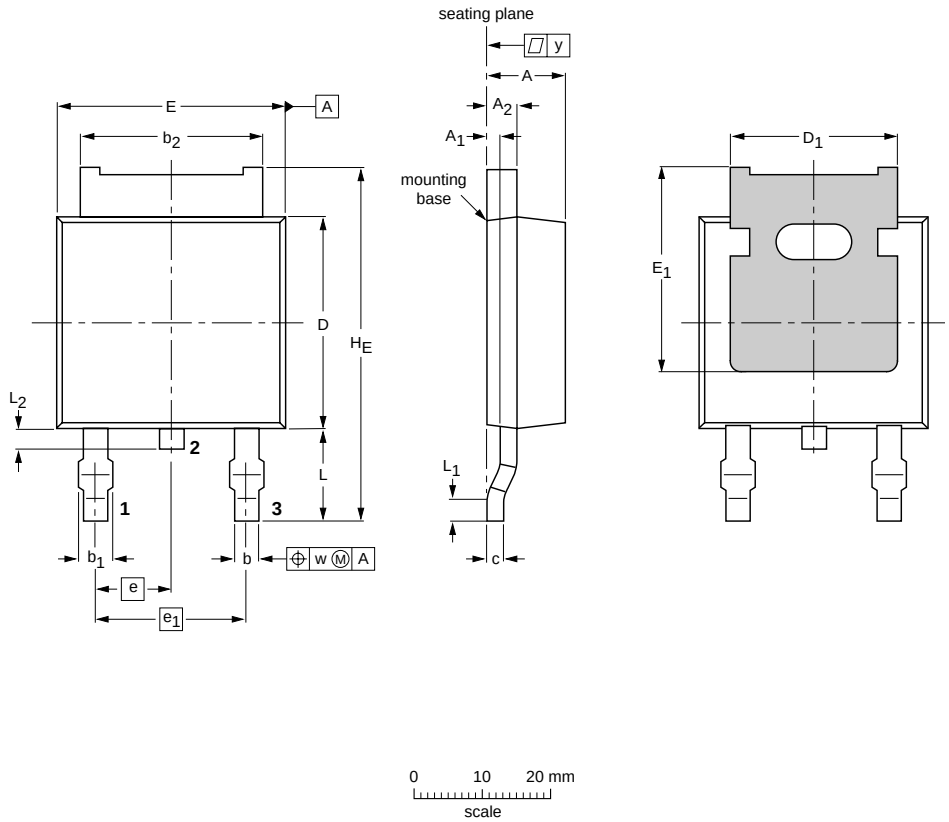
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	V_{IS} = 5 V	-	15	30	µs
t_r	Rise time		-	30	60	µs
$t_{d\ off}$	Turn-off delay time	V_{IS} = 0 V	-	70	140	µs
t_f	Fall time		-	35	70	µs

1 The input voltage below which the overload protection circuits will be reset.

2 Not directly measureable from device terminals.

MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1(1)	A_2	b	b_1 max.	b_2	c	D max.	D_1 max.	E max.	E_1 min.	e	e_1	H_E max.	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.7 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428						98-04-07

Fig.2. SOT428 surface mounting package[1], centre pin connected to mounting base.

1 Epoxy meets UL94 V0 at 1/8". Net mass: 1.1 g
For soldering guidelines and SMD footprint design, please refer to Data Handbook SC18.

DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS[1]	**PRODUCT STATUS**[2]	**DEFINITIONS**
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product
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Limiting values		
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		
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